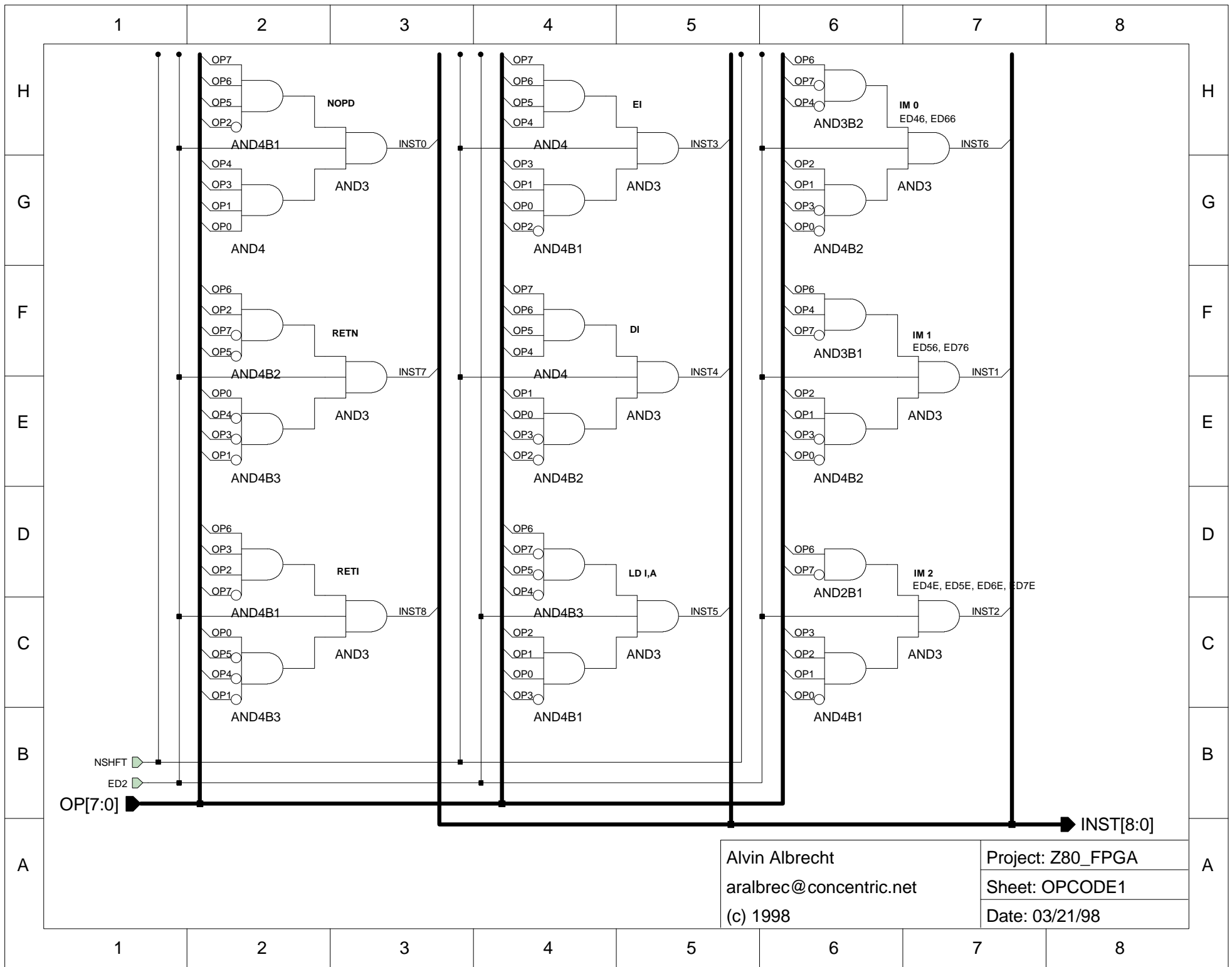


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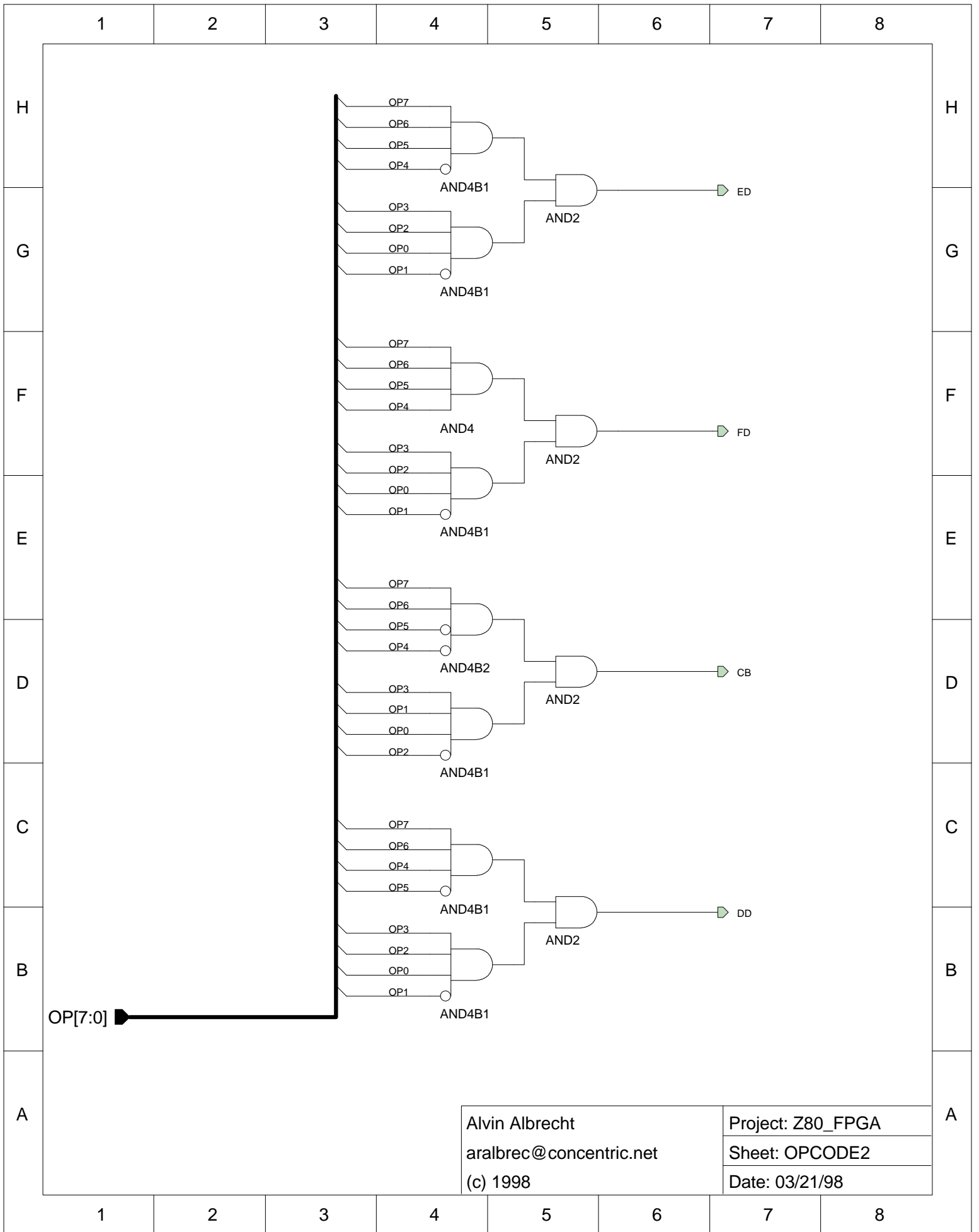
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 (c) 1998

Project: Z80_FPGA
 Sheet: 3/3
 Date: 03/21/98



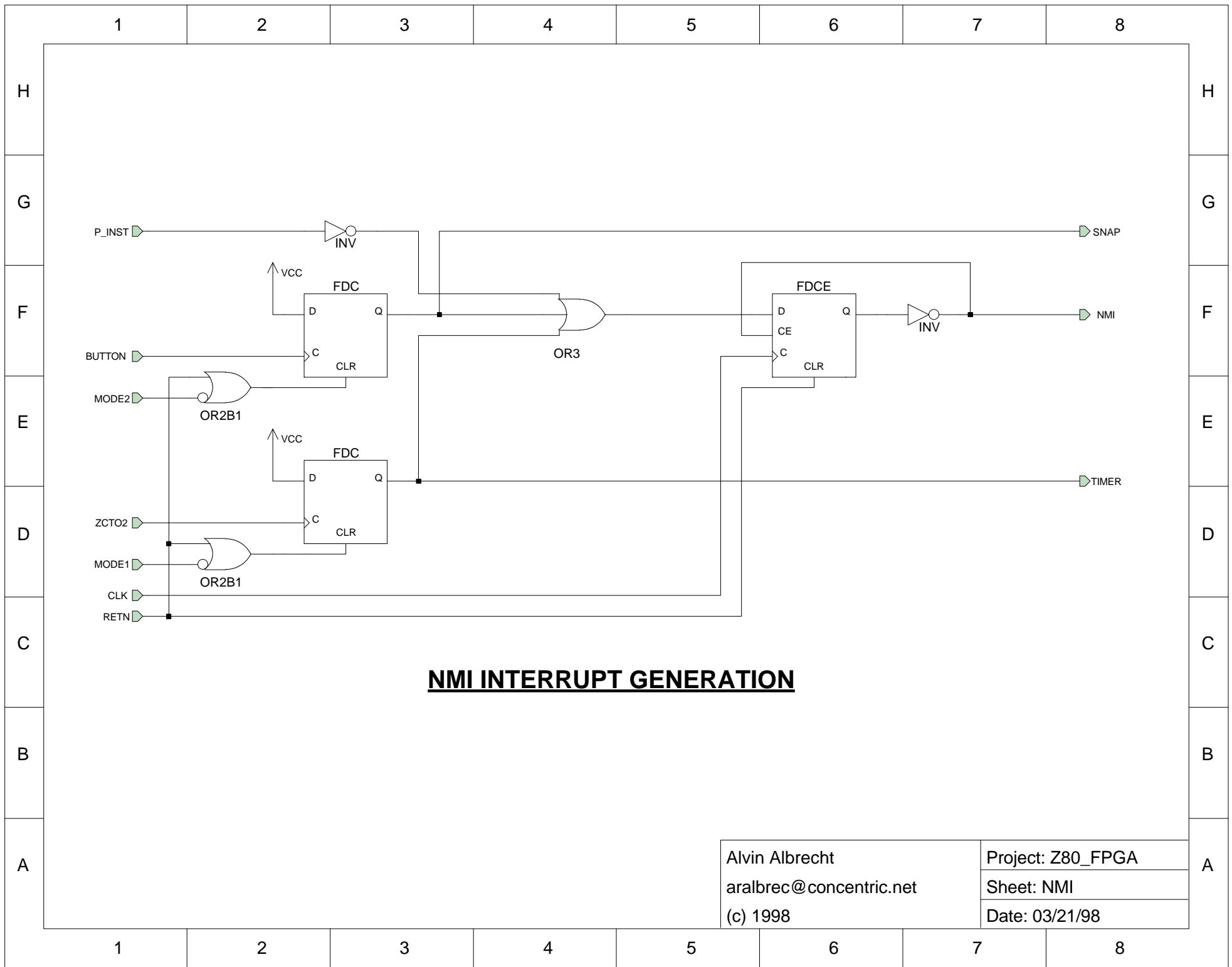
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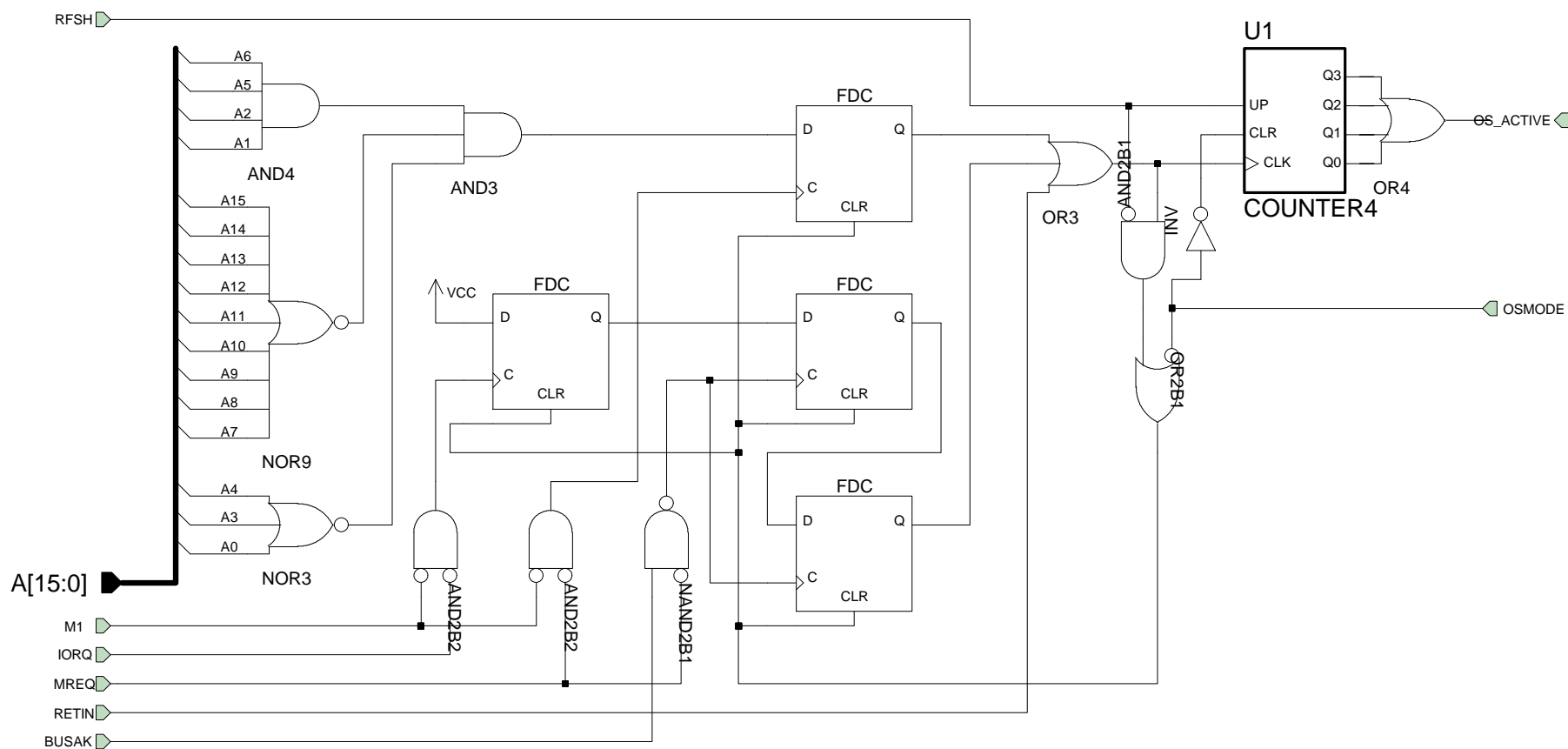
Project: Z80_FPGA
 Sheet: OPCODE2
 Date: 03/21/98



NMI INTERRUPT GENERATION

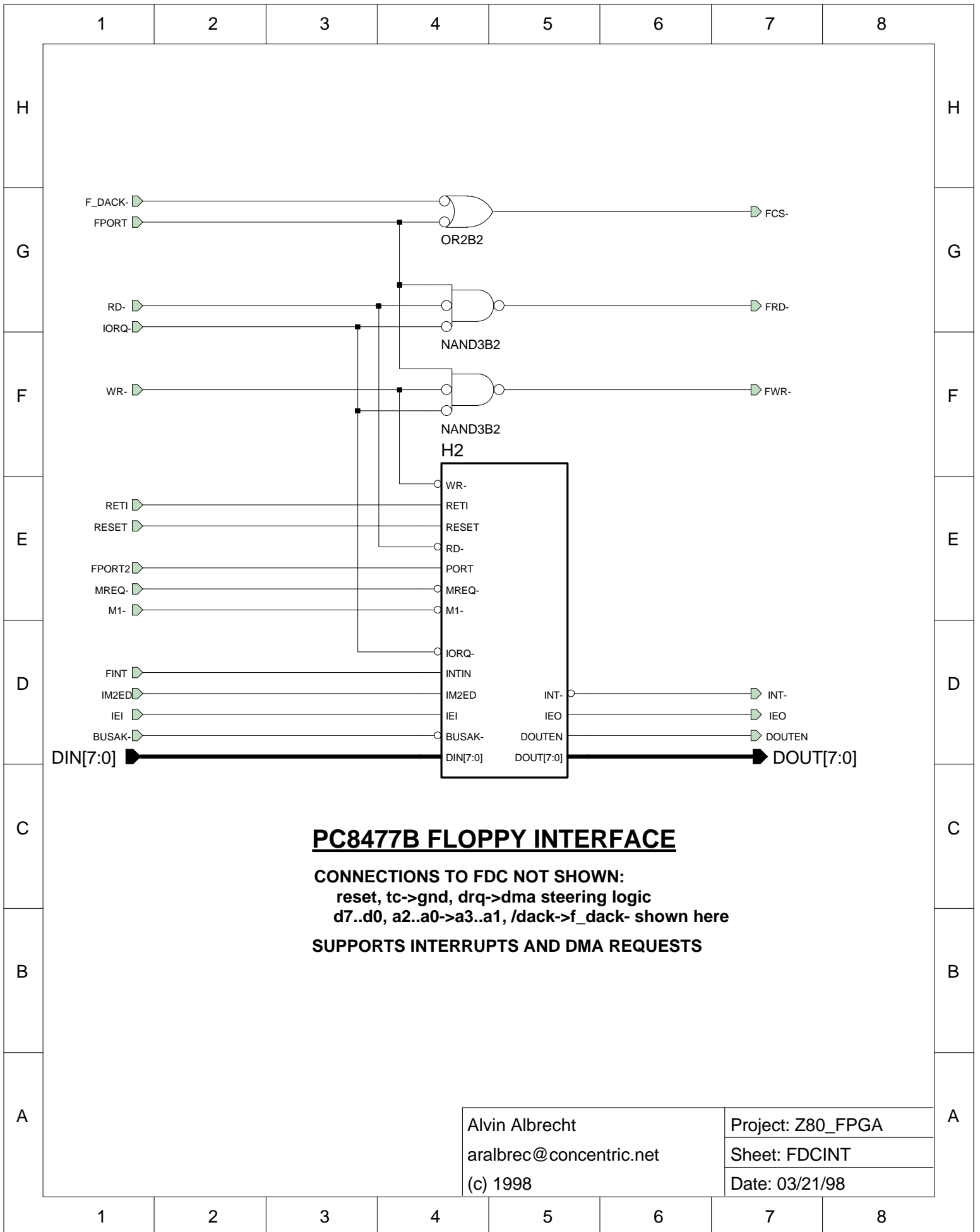
Alvin Albrecht aralbre@concentric.net (c) 1998	Project: Z80_FPGA
	Sheet: NMI
	Date: 03/21/98

OPERATING SYSTEM INTERRUPT CONTROL



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Project: Z80_FPGA
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 Date: 03/21/98



PC8477B FLOPPY INTERFACE

CONNECTIONS TO FDC NOT SHOWN:

reset, tc->gnd, drq->dma steering logic

d7..d0, a2..a0->a3..a1, /dack->f_dack- shown here

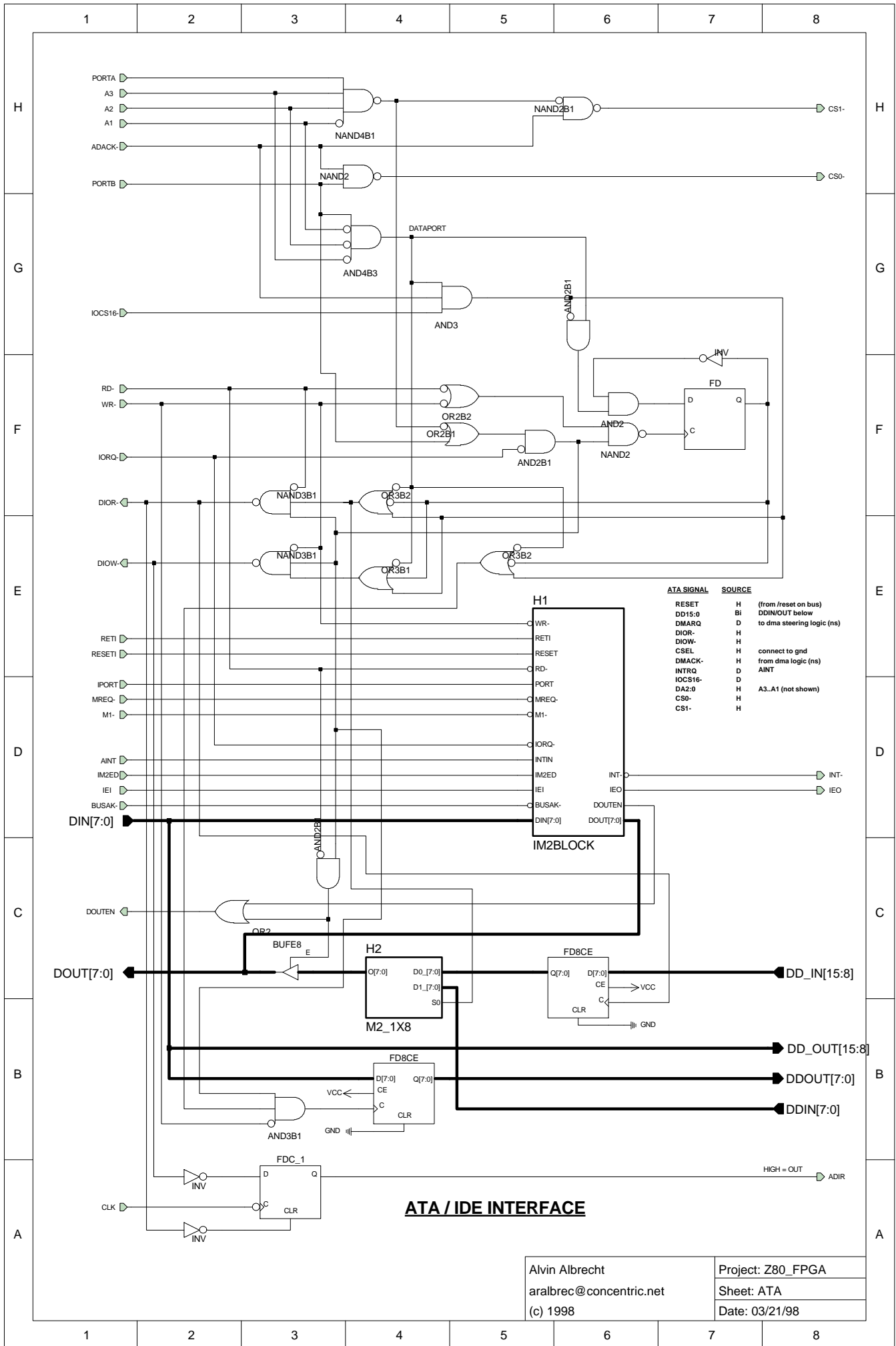
SUPPORTS INTERRUPTS AND DMA REQUESTS

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Project: Z80_FPGA

Sheet: FDCINT

Date: 03/21/98

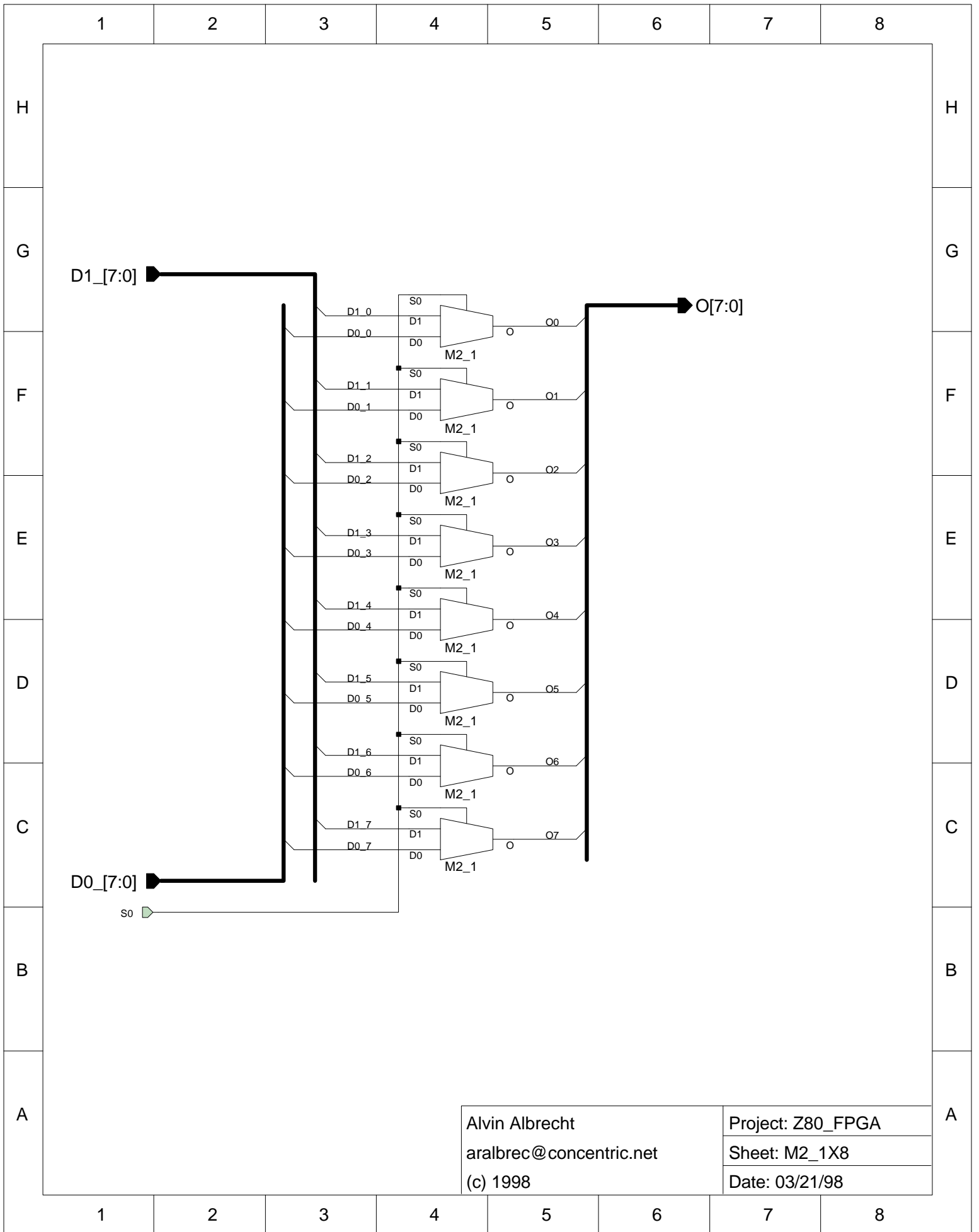


ATA SIGNAL	SOURCE
RESET	H (from /reset on bus)
DD15:0	B1 DDIN/OUT below
DMARQ	D to dma steering logic (ns)
DIOR-	H
DIOW-	H
RETI	H
RESETI	H
DMACK-	H from dma logic (ns)
INTRQ	D AINT
IOCS16-	D
DAZ:0	H A3..A1 (not shown)
CS0-	H
CS1-	H

ATA / IDE INTERFACE

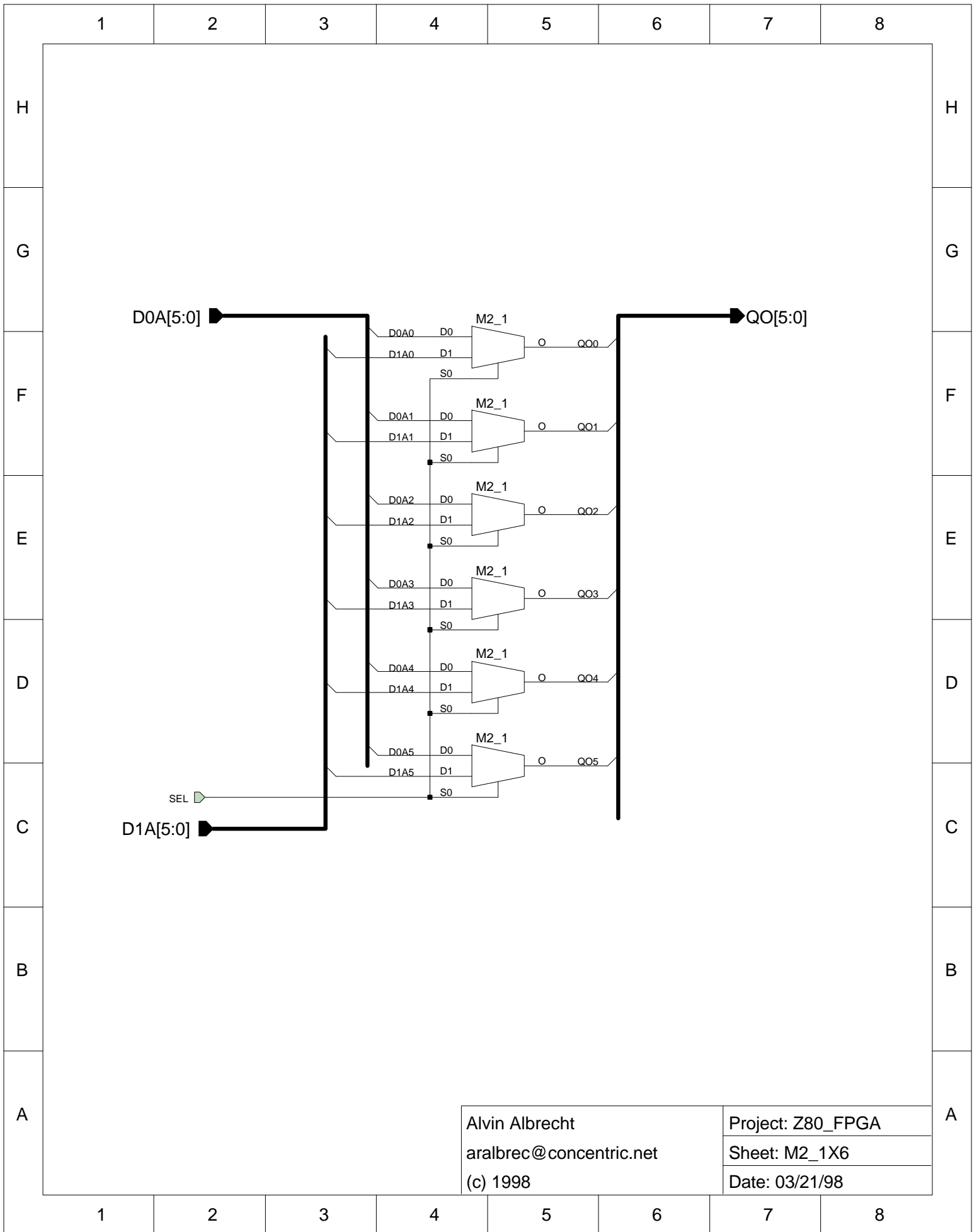
Alvin Albrecht
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Project: Z80_FPGA
 Sheet: ATA
 Date: 03/21/98



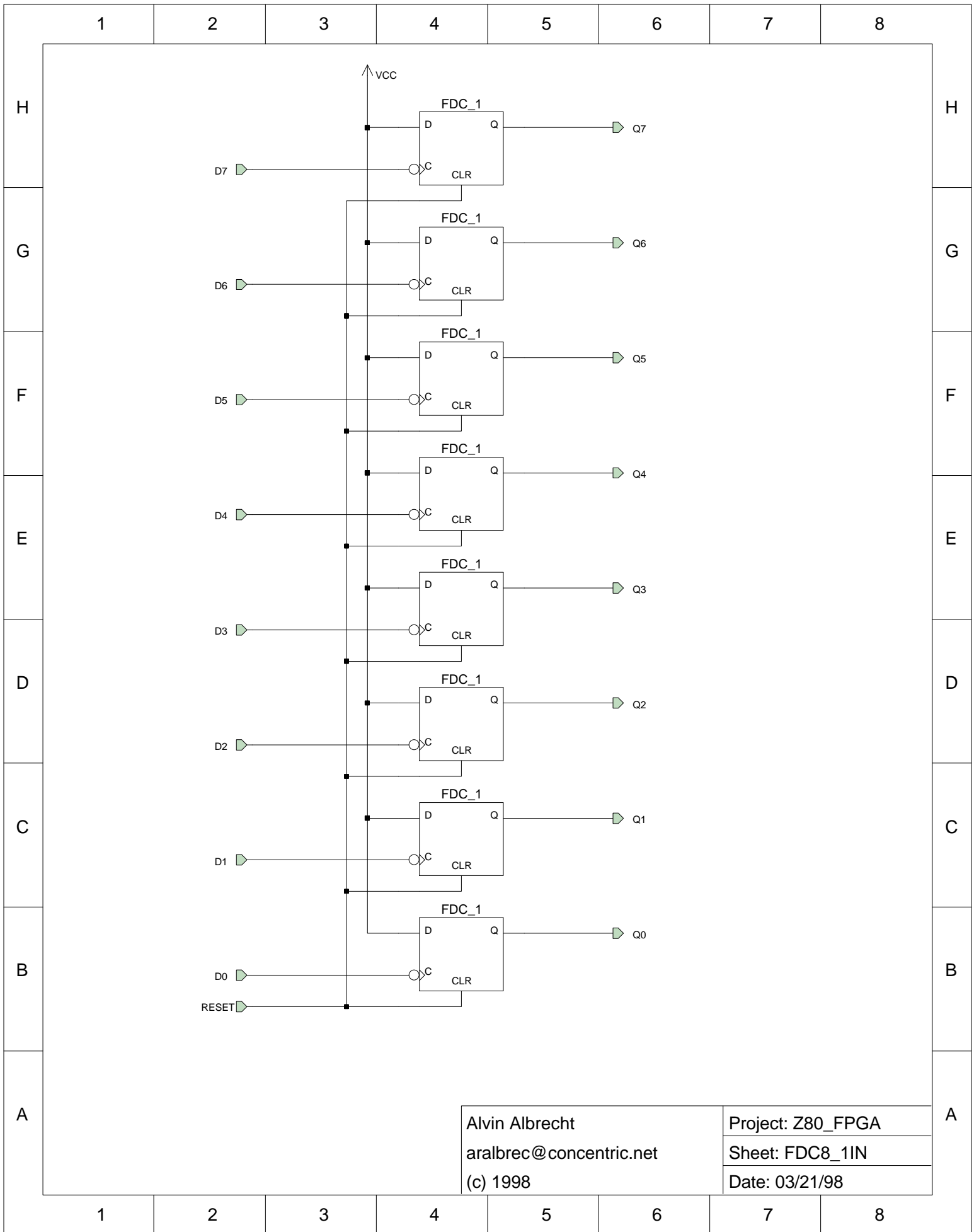
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Project: Z80_FPGA
 Sheet: M2_1X8
 Date: 03/21/98



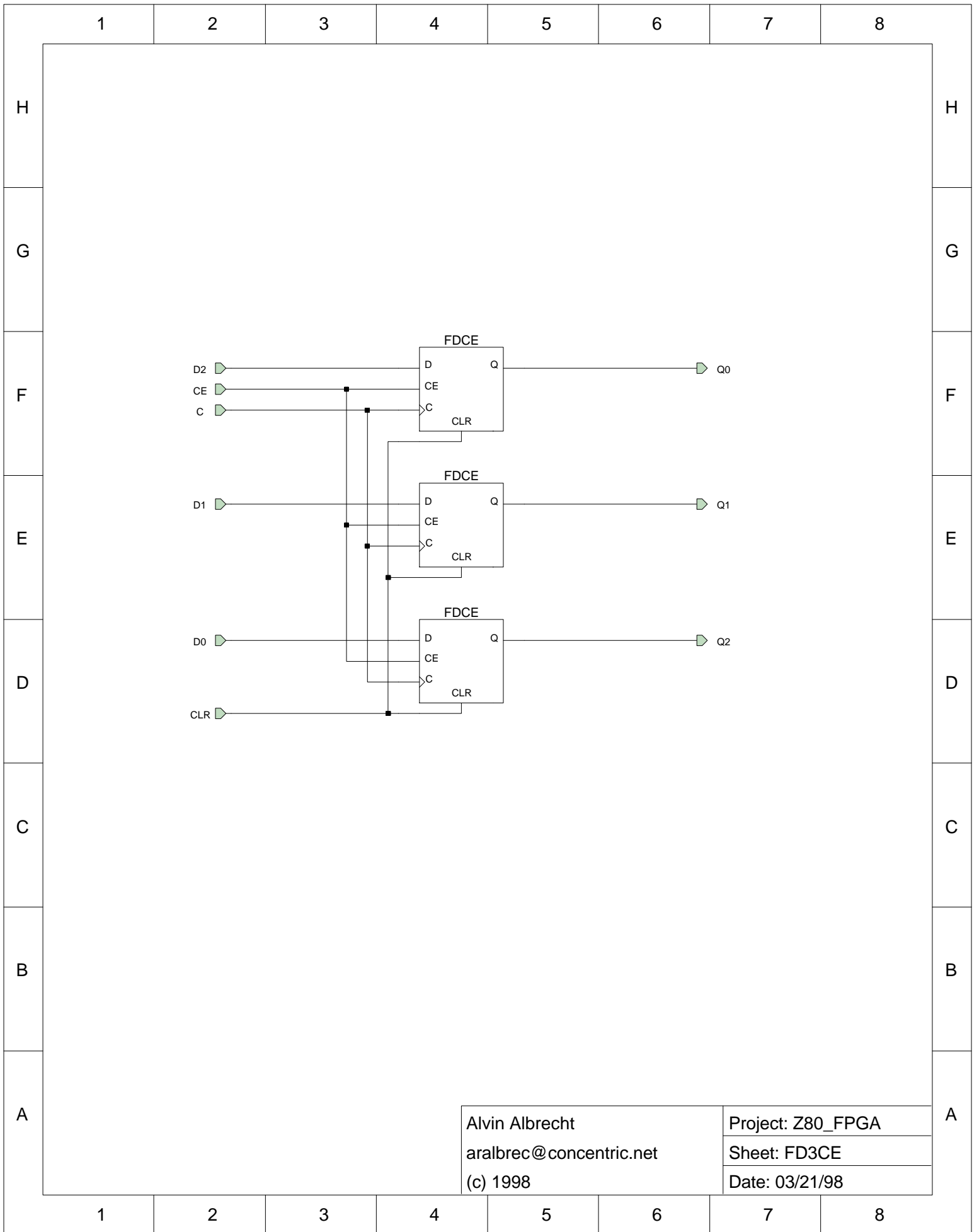
Alvin Albrecht
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Project: Z80_FPGA
 Sheet: M2_1X6
 Date: 03/21/98



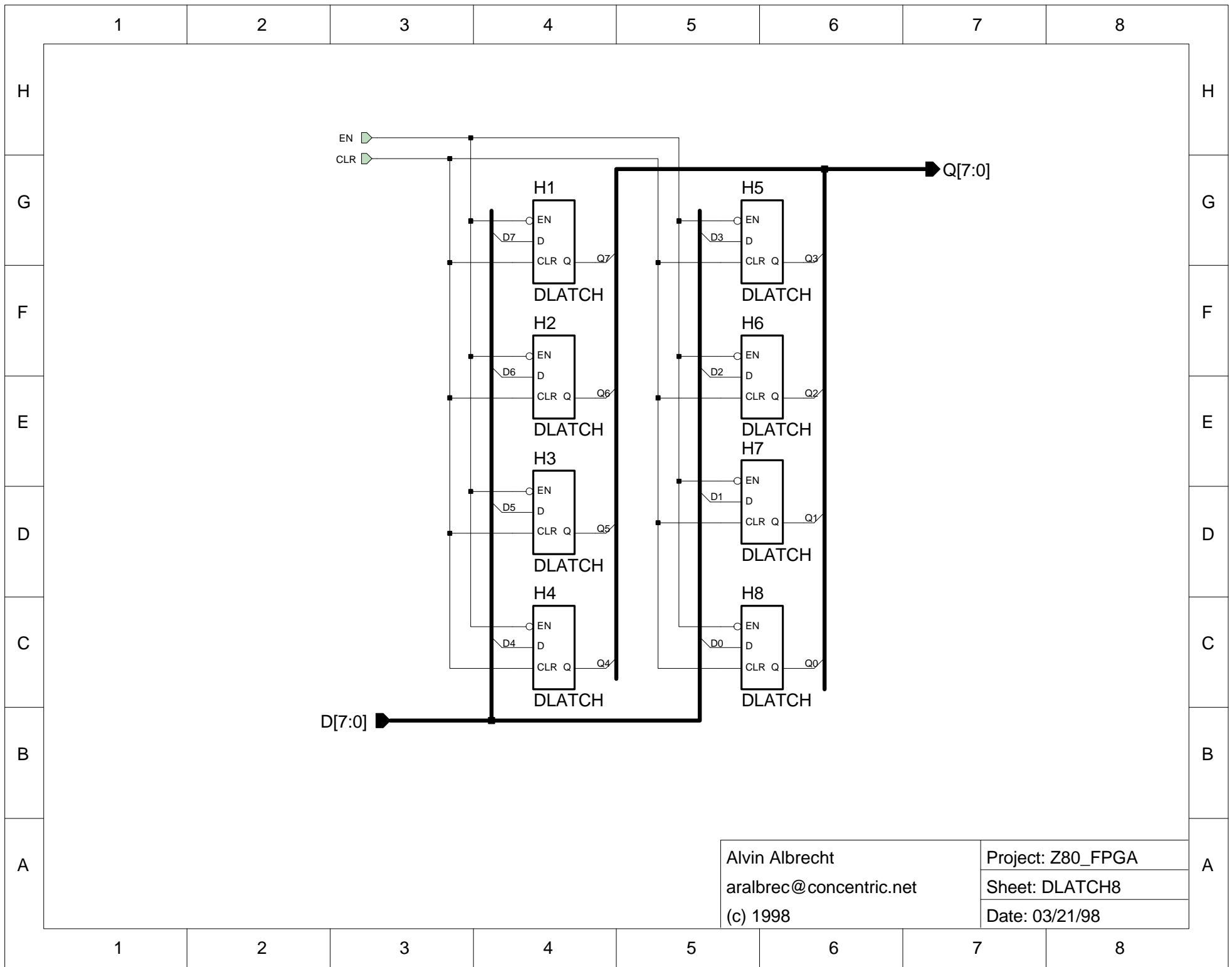
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Project: Z80_FPGA
 Sheet: FDC8_1IN
 Date: 03/21/98

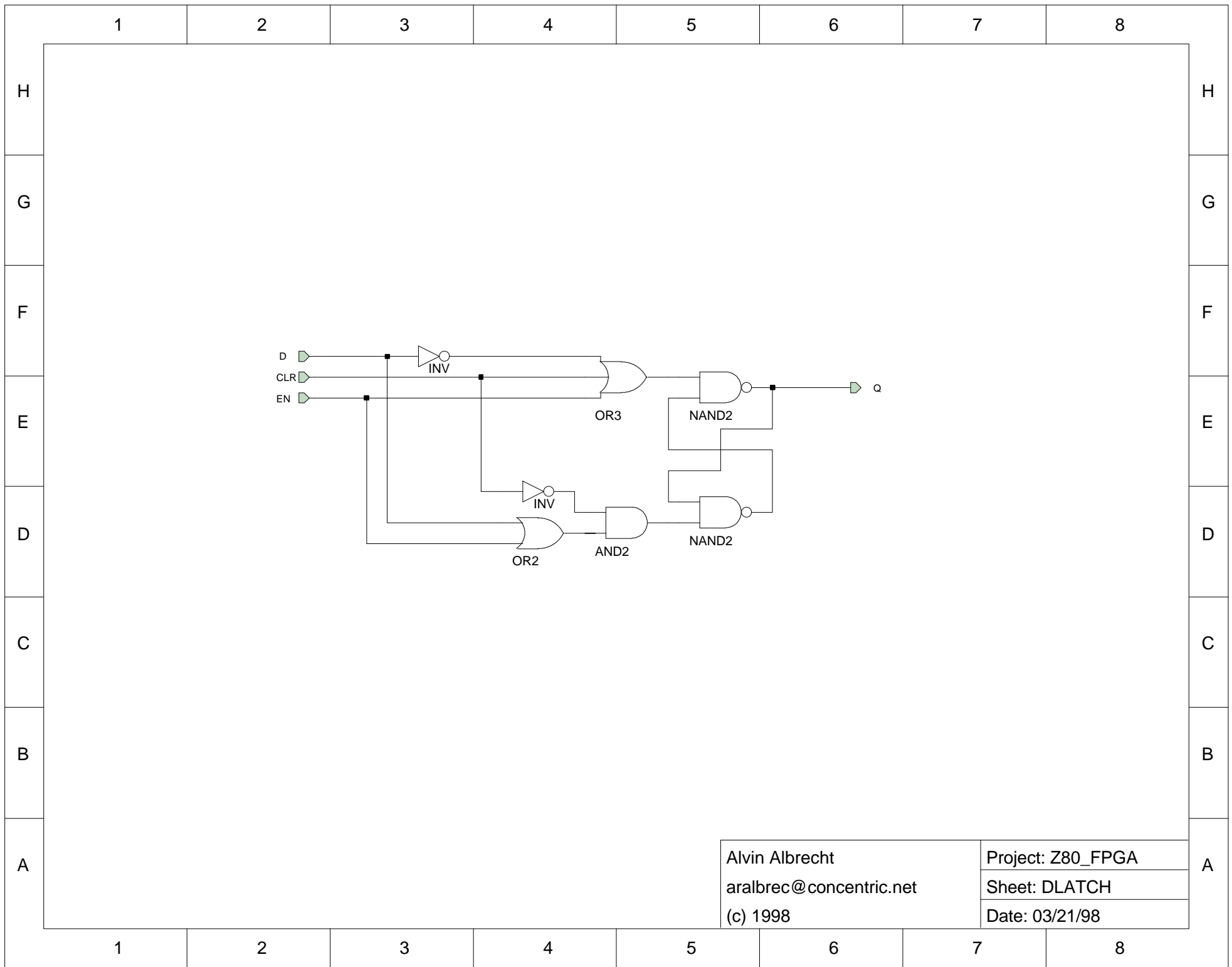


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Project: Z80_FPGA
 Sheet: FD3CE
 Date: 03/21/98

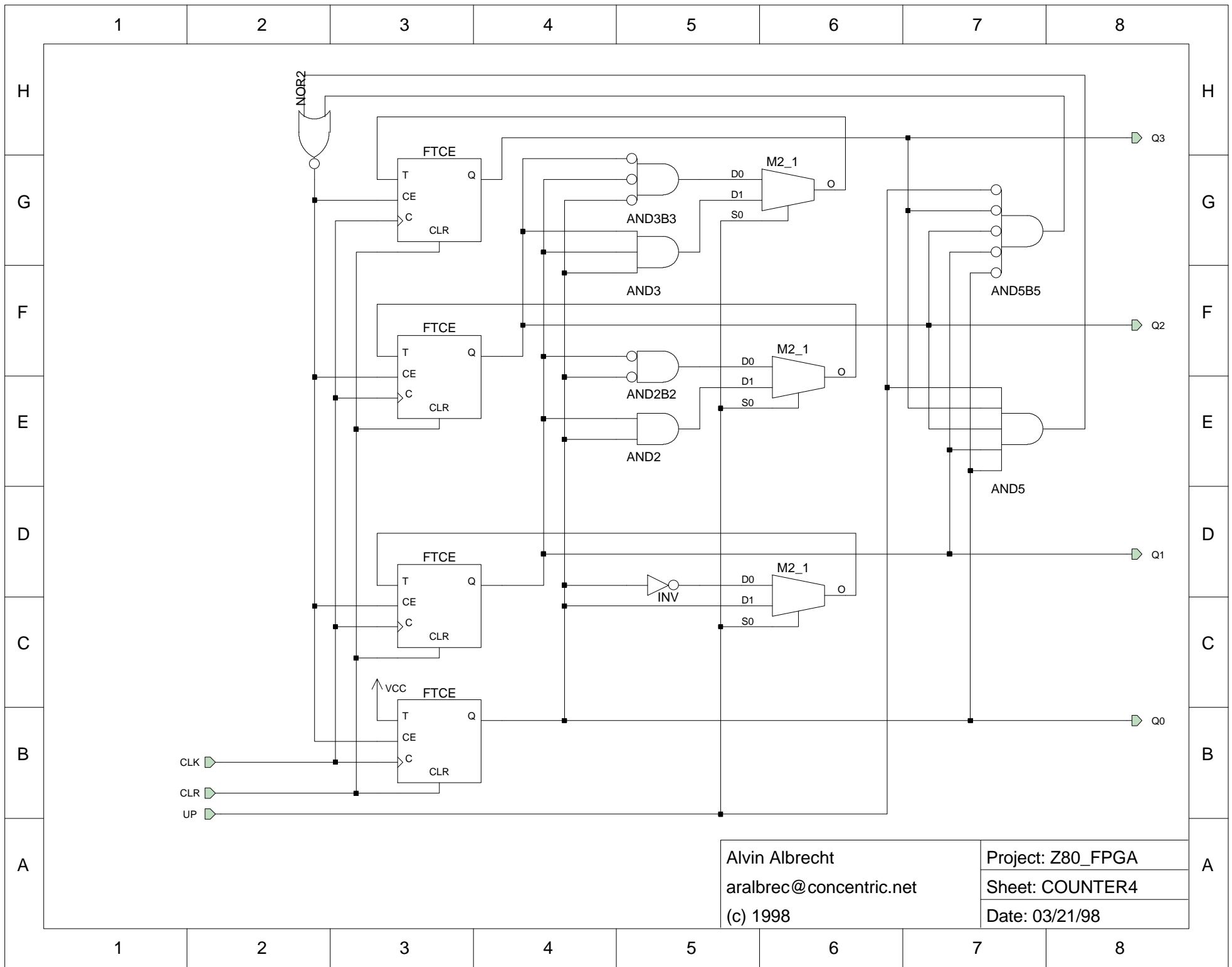


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	Sheet: DLATCH8
	Date: 03/21/98



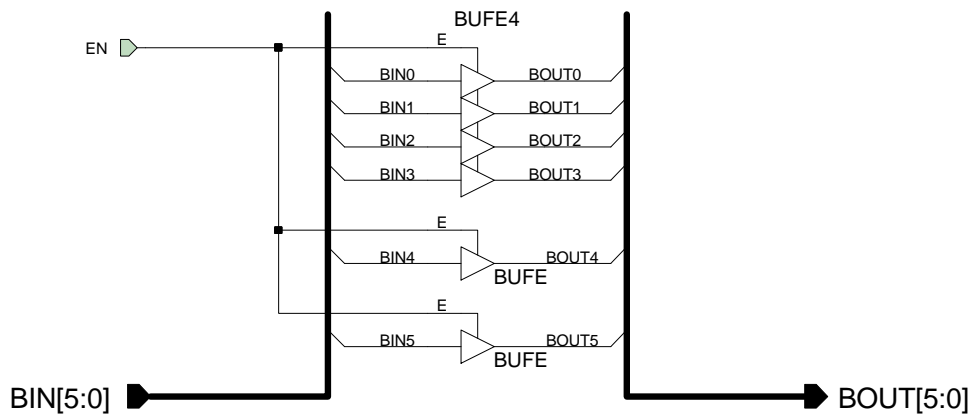
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Project: Z80_FPGA
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 Date: 03/21/98



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Project: Z80_FPGA
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 Date: 03/21/98



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Project: Z80_FPGA
 Sheet: BUFE6
 Date: 03/21/98